a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(2) Kindly rewrite Claim 5 as follows:

5. (Amended)   The semiconductor device as recited in Claim 1 wherein the second portion comprises polysilicon.

(3) Kindly rewrite Claim 7 as follows:

7. (Twice Amended)   A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench, wherein the isolation region includes a first portion and a second post portion located thereover; and

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions

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(4) Kindly rewrite Claim 10 as follows:

B4

10. (Amended)   The semiconductor device as recited in Claim 7 wherein the second

portion comprises polysilicon.

(5) Kindly rewrite Claim 12 as follows:

Sub C3

B5

12. (Twice Amended)   A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent the channel region, the isolation region being located

within a trench formed in the semiconductor substrate and not extending under the channel region

and including a first portion and a second post portion located thereover; and

source/drain regions having a first portion located in the semiconductor substrate and a

second portion located on the isolation region and in contact with the second post portion, but not

in the semiconductor substrate, wherein an interface separates the first and second portions.

(6) Kindly rewrite Claim 17 as follows:

Sub C4

B6

17. (Twice Amended)   A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second

transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench

located within the semiconductor substrate, wherein the isolation region includes a first portion and

a second post portion located thereover; and

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source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(7) Kindly rewrite Claim 21 as follows:

21. (Twice Amended)   A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region within a trench located in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

forming a first portion of one of a source/drain region in the semiconductor substrate and a second portion of the one of the source/drain region on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(8) Kindly rewrite Claim 25 as follows:

25. (Amended)   The method as recited in Claim 21 wherein forming a second portion includes forming a second portion with polysilicon.

(9) Kindly rewrite Claim 27 as follows:

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